CLAIMS

WHAT IS CLAIMED IS:

1. A packet identifier table for use in a re-multiplexer module having an input processor controlled by a host processor in a packet processing system, comprising:

an active table containing values used by the input processor to select packets for storage in a input packet data stream; and

a pending table containing values that can be modified by the host processor while the active table is being used by the input processor.

2. The packet identifier table of claim 1, wherein the packet identifier table is constructed as a multi-port accessible memory.

3. The packet identifier table of claim 2, wherein the multi-port accessible memory is a dual-port accessible memory.

4. The packet identifier table of claim 3, wherein the dual-port accessible memory is partitioned into two portions to form the active table and the pending table.

5. The packet identifier table of claim 1, further including a switching mechanism allowing the host processor to switch the active table into a current pending table and switch the pending table into a current active table.

6. The packet identifier table of claim 5, wherein the switching mechanism includes modifying a control bit in the input processor via the host processor.

7. A packet identifier table for use in a re-multiplexer module having an input processor controlled by a host processor in a packet processing system, comprising:

an active table containing values used by the input processor to select packets for storage in a input packet data stream; and

a pending table containing values that can be modified by the host processor while the active table is being used by the active table,

wherein the packet identifier table is a multi-port accessible memory divided into the active table and pending table, and further including a switching mechanism allowing the host processor to switch the active table into a current pending table and switch the pending table into a current active table by modifying a control bit in the input processor.

8. The packet identifier table of claim 7, wherein the multi-port accessible memory is a dual-port accessible memory.

9. The packet identifier table of claim 8, wherein the dual-port accessible memory is partitioned into two portions to form the active table and the pending table.